FORMING OF CLOSE THIN TRENCHES

PRIORITY CLAIM

[1] This application claims priority from French patent application No. 02/14460, filed November 19, 2002, which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[2] The present invention relates to the forming of close thin trenches in a semiconductor substrate.

DISCUSSION OF THE RELATED ART

[3] The minimum width of a trench and the spacing between trenches conventionally depend on the lithography apparatus used to insolate resists. The more the insolation is accurate, the more possible it is to obtain very narrow trenches after etching.

SUMMARY

[4] When it is not necessarily possible to have a lithography device providing narrow trenches, the described embodiments of the present invention aim at forming trenches having a width smaller than the minimum width normally possible with a given lithography device.

[5] Embodiments of the present invention provide a method for forming narrow trenches in a silicon substrate comprising the steps of etching the substrate to form first trenches separated by first silicon ribs; performing a thermal oxidation of the substrate to form a silicon oxide layer developing inside and outside of the silicon, whereby second trenches narrower than the first trenches and second silicon ribs narrower than the first silicon ribs are obtained; filling the second trenches with fingers of an etchable material; etching the silicon oxide down to the upper surface of the second ribs while keeping silicon oxide portions between said etchable material fingers and the second ribs; etching away the second silicon ribs and said etchable material fingers; etching the silicon oxide for a duration sufficient to expose the substrate at the bottom of the silicon oxide portions, while leaving in place silicon oxide fingers; and

anisotropically etching the substrate between the oxide fingers to form narrow trenches in the substrate.

[6] According to an alternative embodiment of the previously-described method, the filling step includes: depositing a layer of an etchable material totally filling the second trenches and covering the silicon oxide layer; and etching said layer of an etchable material for a duration sufficient to leave in place only fingers in the second trenches.

[7] According to an alternative embodiment of the previously-described method, an additional step of etching back of said silicon oxide fingers is provided.

[8] According to an alternative embodiment of the previously-described method, the method further comprises the steps of: depositing a filling layer formed of a material selectively etchable with respect to the substrate, the filling layer totally filling the narrow trenches and covering the substrate ribs separating the narrow trenches; etching the filling layer to expose the substrate ribs, while keeping the material present between ribs; performing a chemical-mechanical polishing of the upper portion of the ribs; and etching back the material remaining between the ribs.

[9] According to an alternative embodiment of the previously-described method, the width and the spacing of the first trenches are identical and the duration of the thermal oxidation of the substrate is provided to obtain substantially identical narrow trenches.

[10] According to an alternative embodiment of the previously-described method, the etchable material used to fill the second trenches is polysilicon.

[11] According to an alternative embodiment of the previously-described method, the second silicon ribs and the etchable material fingers are etched simultaneously.

[12] The foregoing features and advantages of embodiments of the present invention will be discussed in detail in the following non-limiting description of specific embodiments in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[13] FIGS.. 1 to **9** illustrate successive steps of a narrow trench manufacturing method according to an embodiment of the present invention;

[14] **FIG. 10** shows the real shape of the narrow trenches obtained according to the method of **FIGS. 1** to **9** the present invention; and

[15] **FIGS. 11** to **14** illustrate a specific embodiment of the last steps of a method according to an embodiment of the present invention.

DETAILED DESCRIPTION

[16] The following discussion is presented to enable a person skilled in the art to make and use the invention. Various modifications to the embodiments will be readily apparent to those skilled in the art, and the generic principles herein may be applied to other embodiments and applications without departing from the spirit and scope of the present invention. Thus, the present invention is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed herein.

[17] The drawings are cross-section views of the initial substrate and of the different layers obtained after each of the narrow trench manufacturing steps according to embodiments of the present invention.

[18] **FIG. 1** shows a substrate ***1*** in which are formed trenches ***T1***. These trenches are formed by using a lithography device and a standard etch process enabling at best obtaining patterns having a ***1.2-μm*** width and distance between of ***1.2 μm***. In the illustrated example, trenches ***T1*** having a ***2-μm*** depth have been formed. Trenches ***T1*** are separated by ribs ***S1*** of the substrate.

[19] At the next step, illustrated in **FIG. 2**, a thermal oxidation is performed to form a silicon oxide layer ***2*** having in this example a ***0.6-μm*** thickness. Trenches ***T2*** narrower than initial trenches ***T1*** are obtained. The substrate ribs have uniformly shrunk by approximately ***0.3 μm***, forming substrate ribs ***S2*** narrower than initial substrate ribs ***S1***. Similarly, the bottom of trenches ***T1*** has deepened by ***0.3 μm***. In the end, trenches ***T2*** and ribs ***S2*** all have a width equal to substantially ***0.6 μm*** and are separated by a silicon oxide layer substantially of a ***0.6-μm*** width.

[20] At the next step, illustrated in **FIG. 3**, a silicon layer ***3*** is deposited to form, in this example, polysilicon, to totally fill trenches ***T2*** and cover silicon oxide layer ***2***. The thickness of polysilicon ***3*** above the ribs of substrate ***S2*** is in this example at least equal to ***1.5 μm***.

[21] As an alternative, another material than silicon could be deposited. Preferably, a material that can be etched with a substantially identical speed could be chosen to simplify the part of the method described in relation with **FIG. 6**.

[22] At the next step, illustrated in **FIG. 4**, polysilicon layer ***3*** is selectively etched with respect to silicon oxide, to expose silicon oxide ***2*** covering substrate ribs ***S2***. The etching is then interrupted so that there remain fingers ***4*** of polysilicon layer ***3*** in trenches ***T2***.

[23] At the next step, illustrated in **FIG. 5**, silicon oxide layer ***2*** is etched for a sufficient duration to expose the upper part of ribs ***S2***. The etching is selective to keep polysilicon fingers ***4*** as well as ribs ***S2*** intact. A structure such as shown in **FIG. 5** is then obtained, in which the remaining portions ***5*** of oxide layer ***2*** have a U shape separating fingers ***4*** and ribs ***S2***.

[24] At the next step, illustrated in **FIG. 6**, the silicon is etched to suppress ribs ***S2*** and polysilicon fingers ***4***. The etching is selective to keep the remaining portions ***5*** of oxide layer ***2*** intact. The etch time is provided to completely remove polysilicon fingers ***4*** and for the etching to approximately stop at the level of the base of silicon ribs ***S2***.

[25] An additional etch step may possibly be provided in the case where the material deposited in trenches ***T2*** cannot be etched according to the method used to etch ribs ***S2***. The additional etch step will however have to be a selective etching with respect to oxide layer ***2***.

[26] At the next step illustrated in **FIG. 7**, an anisotropic etching of the silicon oxide is performed in selective fashion with respect to silicon, for a duration enabling exposing substrate ***1*** at the bottom of the remaining U-shaped silicon oxide portions *5* while leaving silicon oxide fingers 6 in place. In the context of the numerical example given hereabove, the etching time is provided to etch approximately ***0.6 μm*** of silicon oxide.

[27] At the next step, illustrated in **FIG. 8**, an anisotropic etching of the portions of substrate ***1*** unprotected by silicon oxide fingers 6 is performed.

[28] At the next step, illustrated in **FIG. 9**, silicon oxide fingers ***6*** are removed.

[29] Narrow trenches ***T3*** having a width of approximately ***0.6 μm*** separated by ribs ***S3*** also having a width of approximately ***0.6 μm*** are thus obtained.

[30] Thus, based on a structure of trenches formed with a minimum ***1.2-μm*** step, it is possible to obtain a structure comprising twice as many trenches with a ***0.6-μm*** step.

[31] Generally, the method of this embodiment of the present invention enables, based on a trench structure formed with a minimum step corresponding to a given lithography device, to obtain a structure comprising twice as many trenches with a step which is twice as small.

[32] It could further be provided to repeat the described method to obtain twice as many trenches with a ***0.3-μm*** step and so on.

[33] As illustrated in **FIG. 10**, in practice, at the step described in relation with **FIG. 9**, it is not the perfectly regular square shape illustrated in **FIG. 9** which is obtained, but rather an irregular shape such as illustrated in **FIG. 10**. The upper surface of ribs ***S3*** is neither a horizontal plane, nor a planar surface, but may exhibit protruding edges. In the case, for example, where capacitors having a dielectric formed of a thin layer uniformly covering the entire surface of the structure of **FIG. 10** are desired to be formed, such surface irregularities may pose problems. It is then provided to level the upper surface of ribs ***S3***, for example, according to the method illustrated in relation with **FIGS. 11** to **14**.

[34] In a preliminary step, illustrated in **FIG. 11**, an oxide layer 8 is deposited to totally fill narrow trenches ***T3*** and cover ribs ***S3***. The oxide thickness is in this example equal to ***0.4 μm***.

[35] At the next step, illustrated in **FIG. 12**, a dry anisotropic etch of oxide ***8*** is performed to expose the upper portion of ribs ***S3*** while keeping the oxide in narrow trenches ***T3***.

[36] As an alternative, oxide layer ***8*** may be replaced with a material that can be selectively etched with respect to the substrate.

[37] At the next step, illustrated in **FIG. 13**, a chemical-mechanical polishing is performed to level the upper portion of the structure.

[38] At the final next step, illustrated in **FIG. 13**, oxide 8 is removed. Narrow trenches ***T3*** separated with ribs ***S2*** having a totally planar upper surface are then obtained.

[39] Trenches formed according to the embodiments of the present invention depicted in **FIGS. 1 – 14** may be utilized in a variety of integrated circuits, such as memory devices where the trenches may, for example, be utilized in forming capacitor structures. Such an integrated circuit may be contained in a variety of diferent types of electronic systems, such as a computer system.

[40] Of course, the present invention is likely to have various alterations, modifications, and improvements which will readily occur to those skilled in the art. In particular, it will be within the abilities of those skilled in the art to define the oxide and polysilicon thicknesses as well as the duration of the etching thereof according to the width, the spacing, and the depth of the desired narrow trenches.

[41] Such alterations, modifications, and improvements are intended to be part of this disclosure, and are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended to be limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.